

FIG. 1

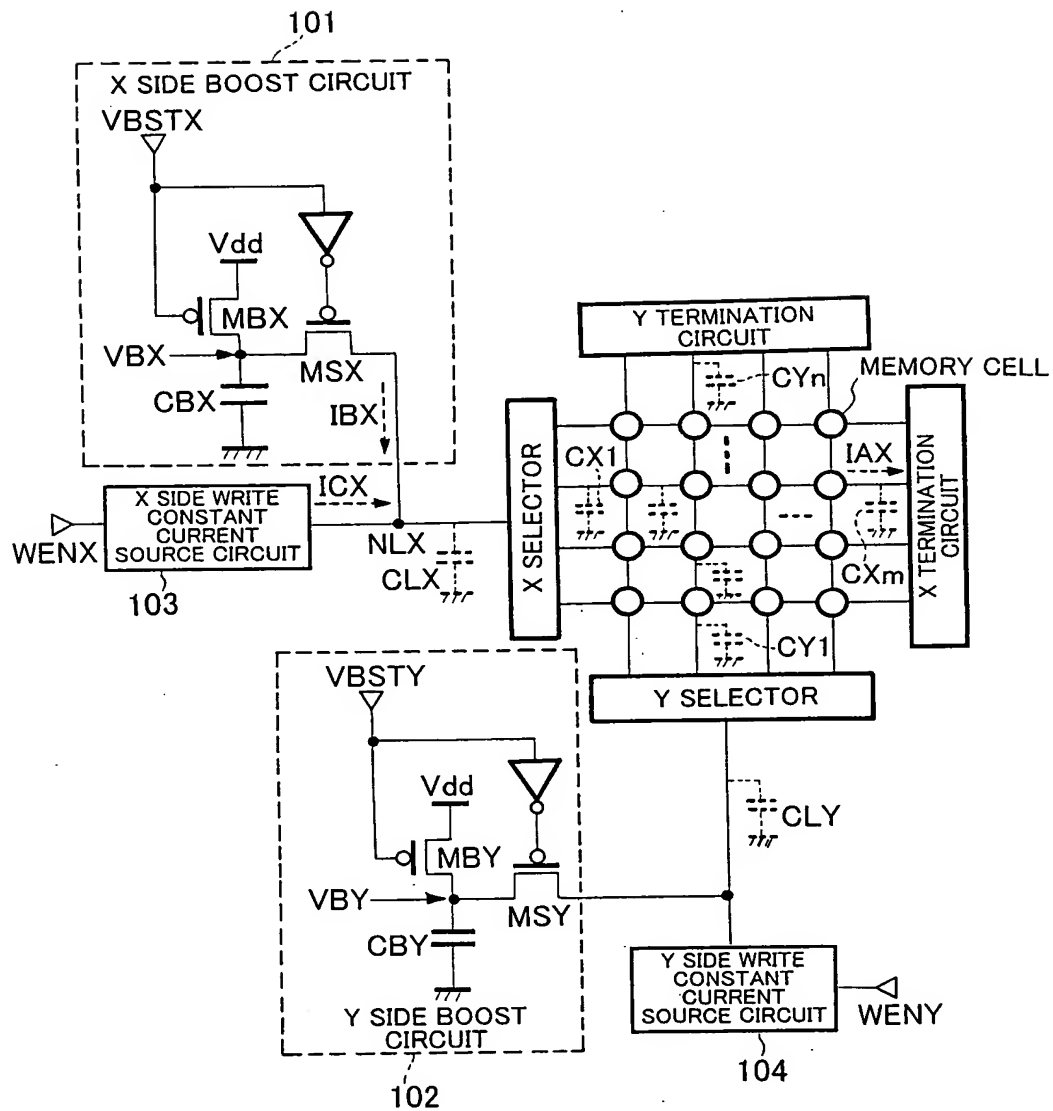


FIG. 2

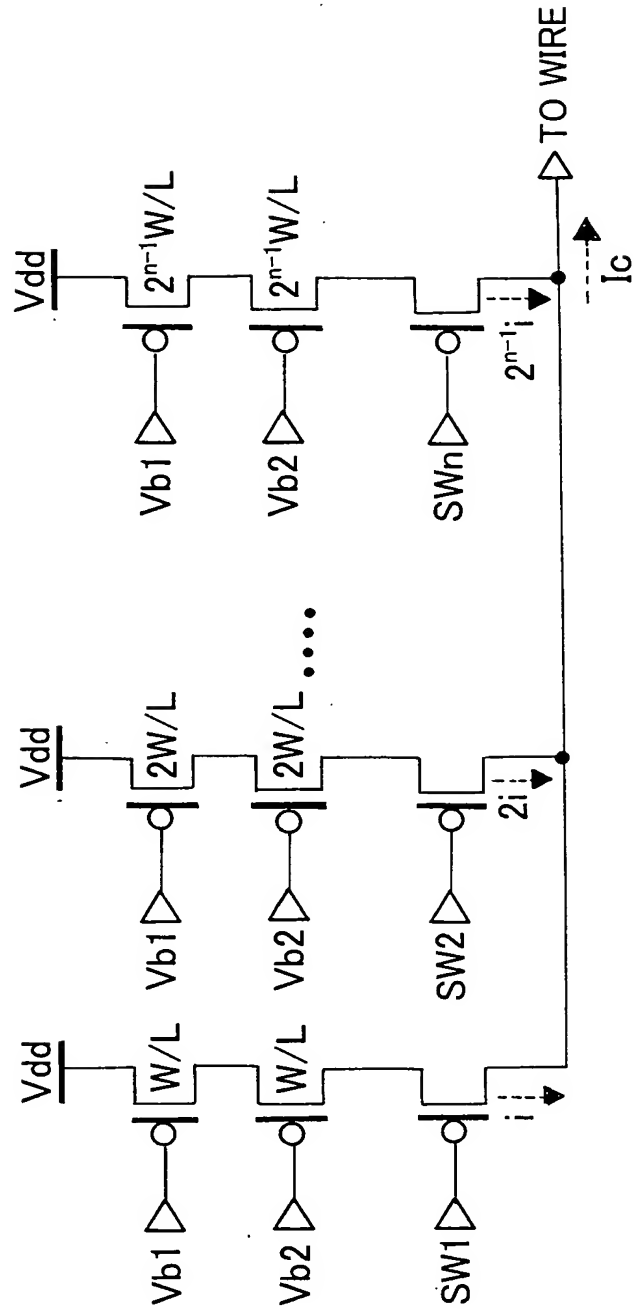


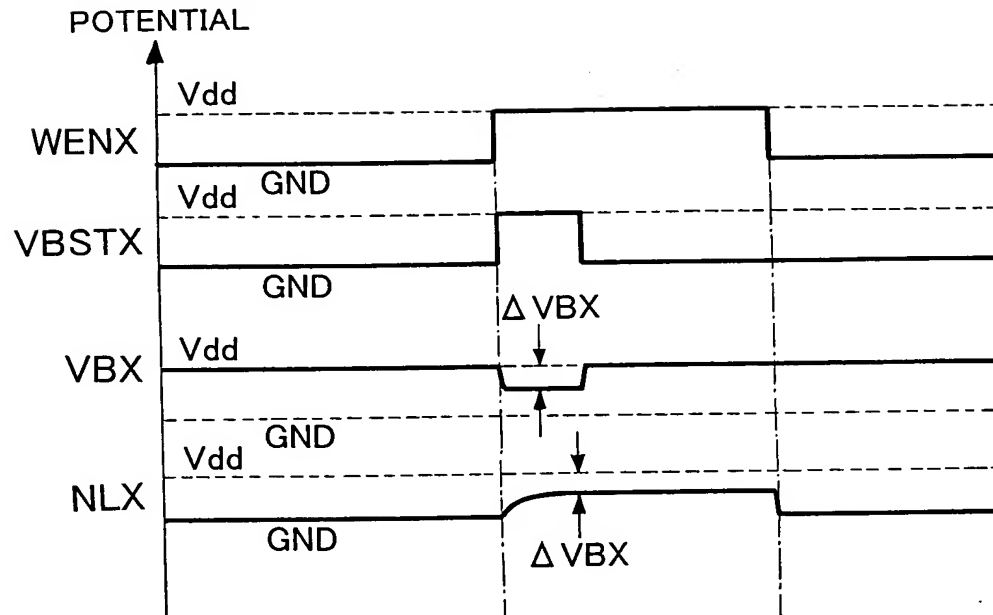
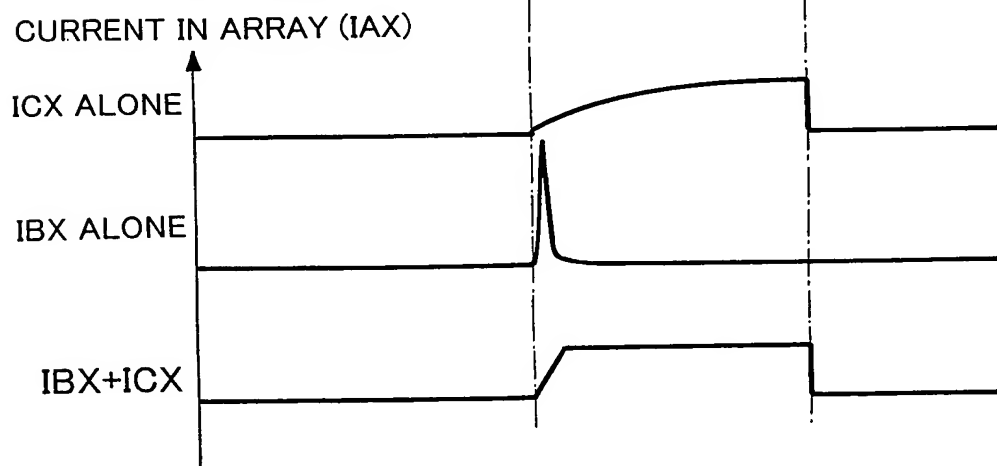
FIG. 3A**FIG. 3B**

FIG. 4A BOOST CIRCUIT

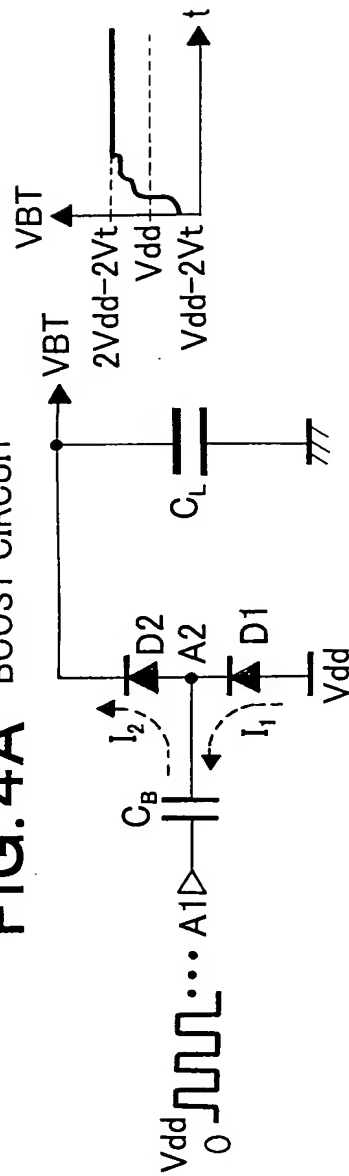


FIG. 4B LEVEL SHIFT CIRCUIT

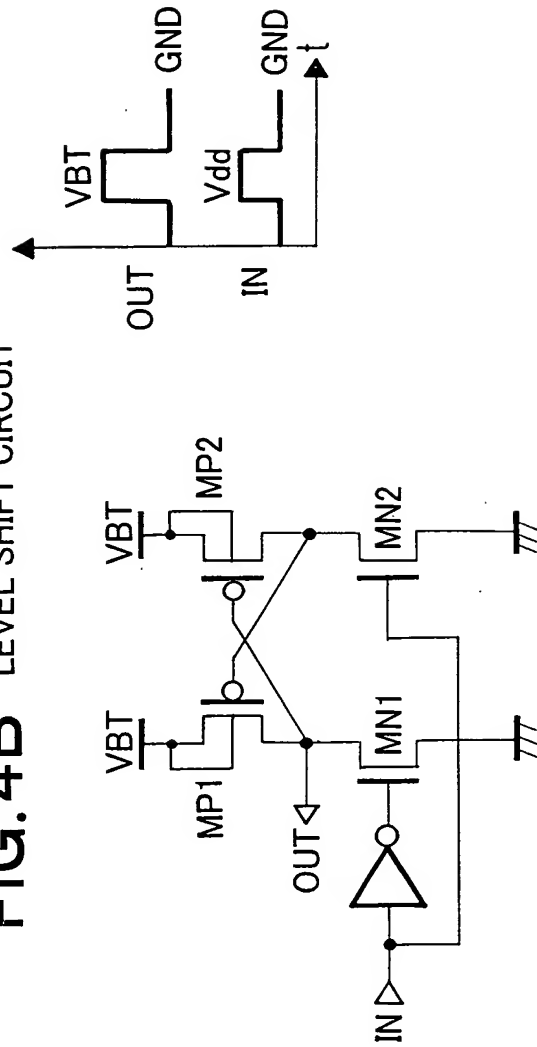


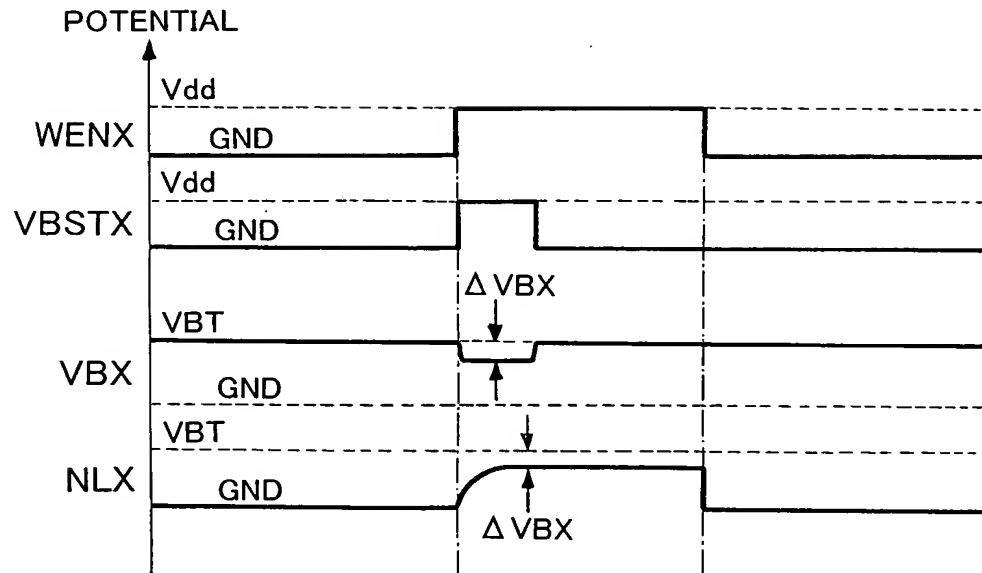
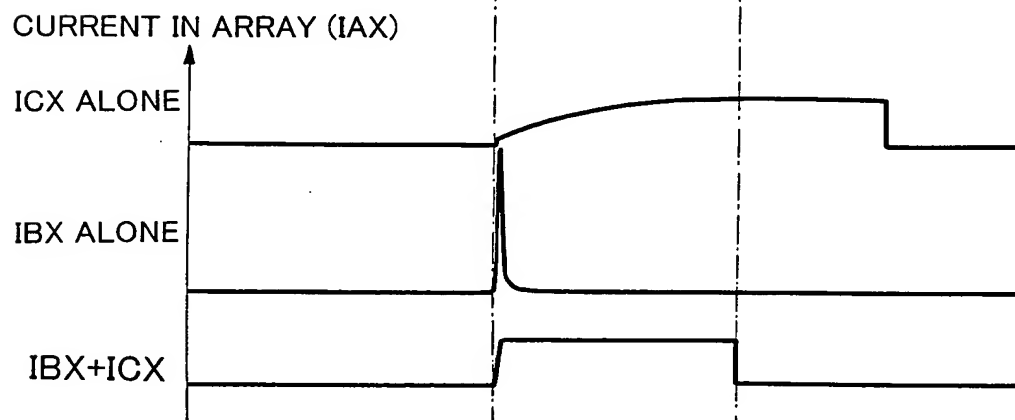
FIG. 6A**FIG. 6B**

FIG. 7

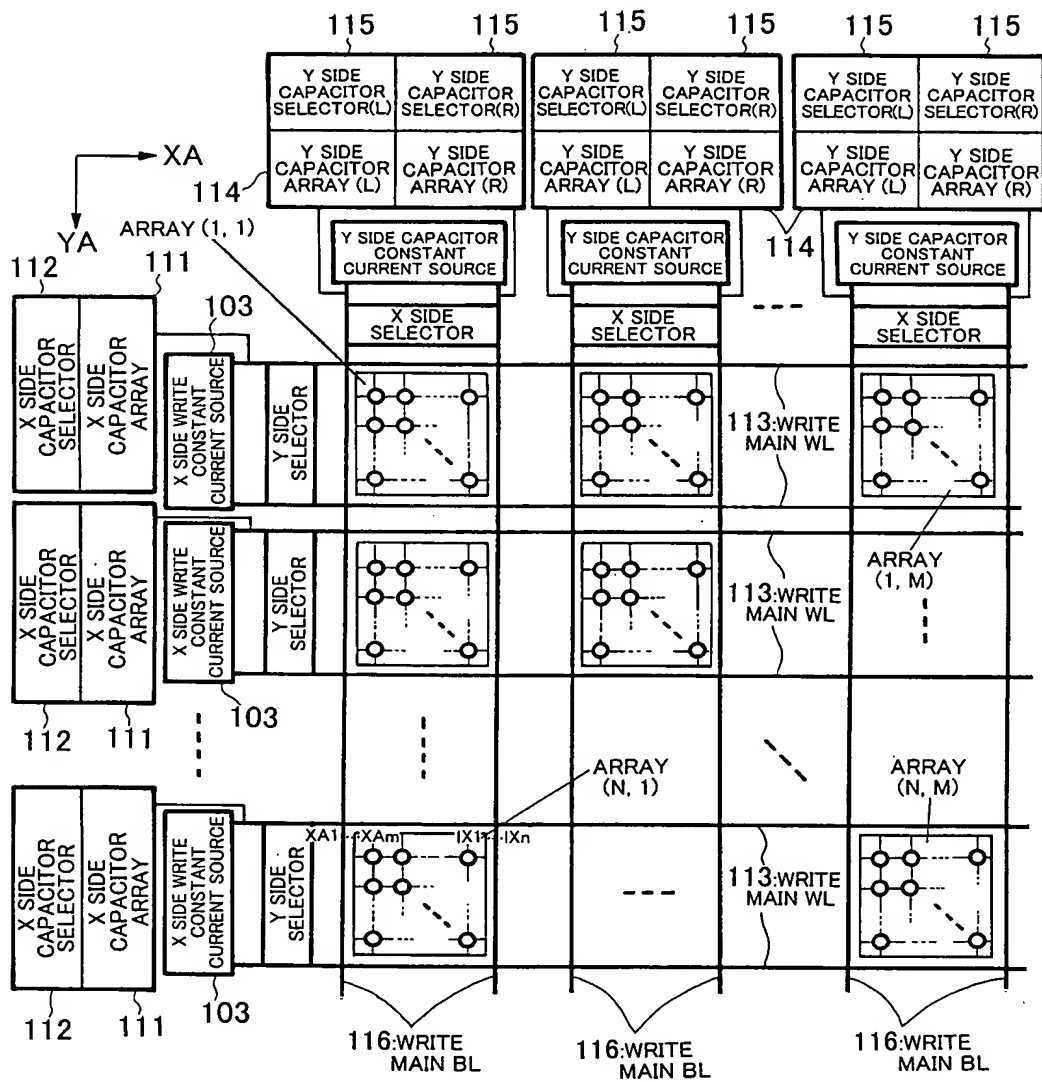


FIG.8

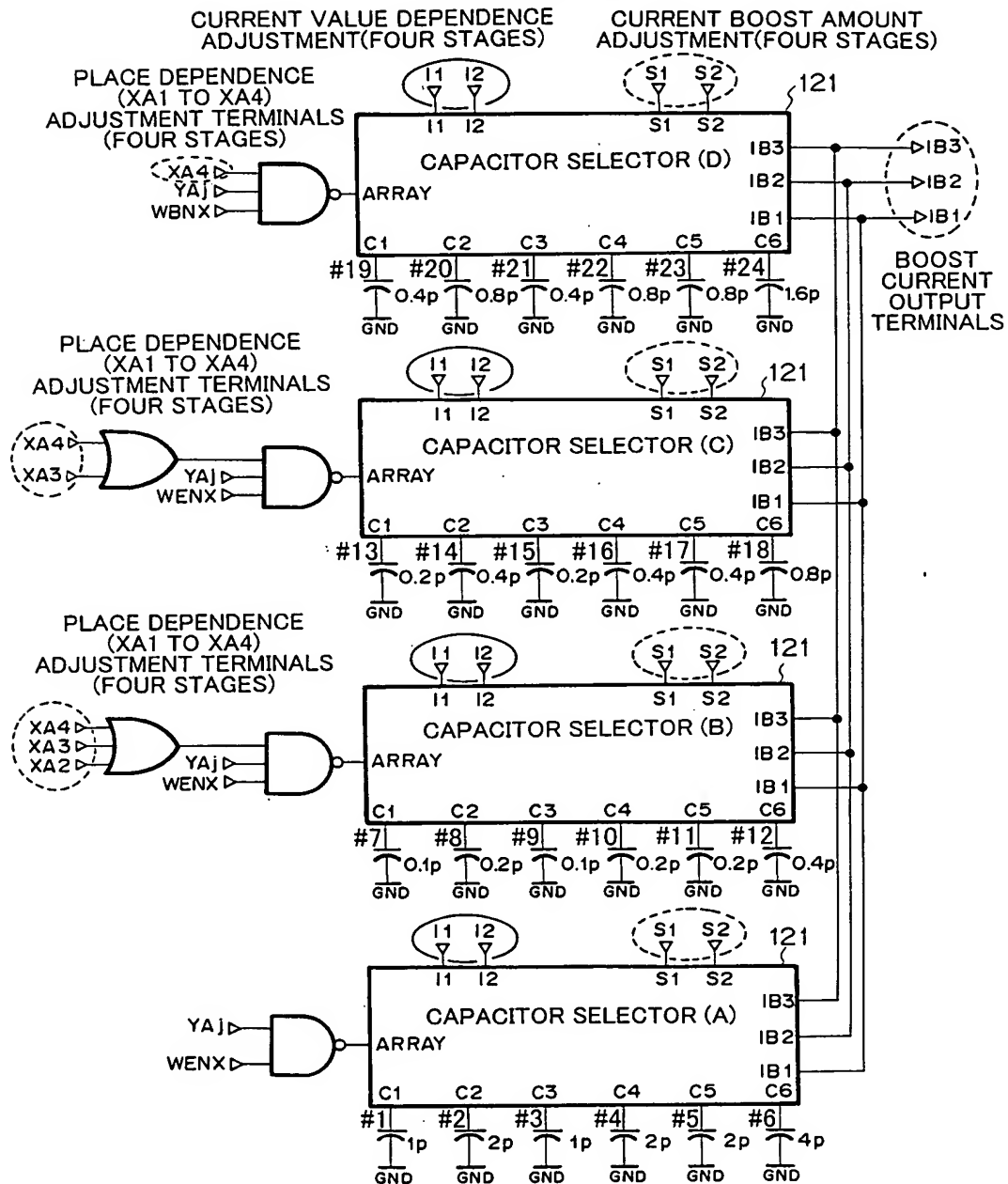


FIG. 10

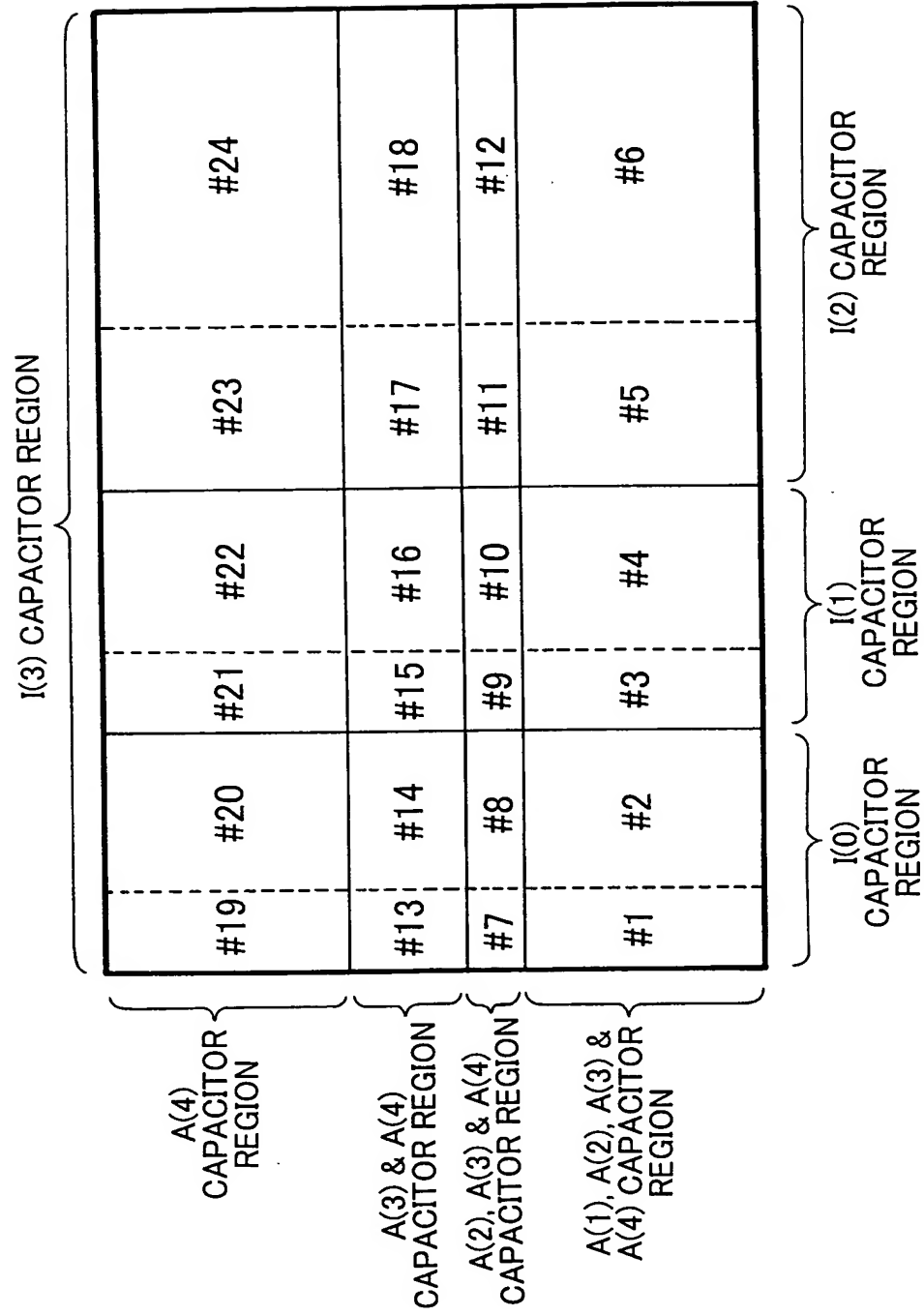


FIG. 11

	CURRENT (3:0)	ARRAY (4:1)	ADJUST- MENT (3:0)	CAPACI- TANCE (PF)	CAPACITORS TO BE USED
1	I(0)	A(1)	S(0)	0.0	NOTHING
2	I(0)	A(1)	S(1)	1.0	#1
3	I(0)	A(1)	S(2)	2.0	#2
4	I(0)	A(1)	S(3)	3.0	#1,#2
5	I(0)	A(2)	S(0)	0.0	NOTHING
6	I(0)	A(2)	S(1)	1.1	#1,#7
7	I(0)	A(2)	S(2)	2.2	#2,#8
8	I(0)	A(2)	S(3)	3.3	#1,#2,#7,#8
9	I(0)	A(3)	S(0)	0.0	NOTHING
10	I(0)	A(3)	S(1)	1.3	#1,#7,#13
11	I(0)	A(3)	S(2)	2.6	#2,#8,#14
12	I(0)	A(3)	S(3)	3.9	#1,#2,#7,#8,#13,#14
13	I(0)	A(4)	S(0)	0.0	NOTHING
14	I(0)	A(4)	S(1)	1.5	#1,#7,#13,#19
15	I(0)	A(4)	S(2)	3.0	#2,#8,#14,#20
16	I(0)	A(4)	S(3)	4.5	#1,#2,#7,#8,#13,#14,#19,#20
17	I(1)	A(1)	S(0)	0.0	NOTHING
18	I(1)	A(1)	S(1)	2.0	#1,#3
19	I(1)	A(1)	S(2)	4.0	#2,#4
20	I(1)	A(1)	S(3)	6.0	#1-#4
21	I(1)	A(2)	S(0)	0.0	NOTHING
22	I(1)	A(2)	S(1)	2.2	#1,#3,#7,#9
23	I(1)	A(2)	S(2)	4.4	#2,#4,#8,#10
24	I(1)	A(2)	S(3)	6.6	#1,#2,#7,#8
25	I(1)	A(3)	S(0)	0.0	NOTHING
26	I(1)	A(3)	S(1)	2.6	#1,#3,#7,#9,#13,#15
27	I(1)	A(3)	S(2)	5.2	#2,#4,#8,#10,#14,#16
28	I(1)	A(3)	S(3)	7.8	#1-#4,#7-#10,#13-#16
29	I(1)	A(4)	S(0)	0.0	NOTHING
30	I(1)	A(4)	S(1)	3.4	#1,#3,#7,#9,#13,#15,#19,#21
31	I(1)	A(4)	S(2)	7.8	#2,#4,#8,#10,#14,#16,#20,#22
32	I(1)	A(4)	S(3)	11.2	#1-#4,#7-#10,#13-#16,#19-#22
33	I(2)	A(1)	S(0)	0.0	NOTHING
34	I(2)	A(1)	S(1)	3.0	#1,#5
35	I(2)	A(1)	S(2)	6.0	#2,#6
36	I(2)	A(1)	S(3)	9.0	#1,#2,#5,#6
37	I(2)	A(2)	S(0)	0.0	NOTHING
38	I(2)	A(2)	S(1)	3.3	#1,#5,#7,#11
39	I(2)	A(2)	S(2)	6.6	#2,#6,#8,#12
40	I(2)	A(2)	S(3)	9.9	#1,#2,#5,#6,#7,#8,#11,#12
41	I(2)	A(3)	S(0)	0.0	NOTHING
42	I(2)	A(3)	S(1)	3.9	#1,#5,#7,#11,#13,#17
43	I(2)	A(3)	S(2)	7.8	#2,#6,#8,#12,#14,#18
44	I(2)	A(3)	S(3)	11.7	#1,#2,#5-#8,#11-#14,#17,#18
45	I(2)	A(4)	S(0)	0.0	NOTHING
46	I(2)	A(4)	S(1)	5.1	#1,#5,#7,#11,#13,#17,#19,#23
47	I(2)	A(4)	S(2)	10.2	#2,#6,#8,#12,#14,#18,#20,#24
48	I(2)	A(4)	S(3)	15.3	#1,#2,#5-#8,#11-#14,#17-#20,#23,#24
49	I(3)	A(1)	S(0)	0.0	NOTHING
50	I(3)	A(1)	S(1)	4.0	#1,#3,#5
51	I(3)	A(1)	S(2)	8.0	#2,#4,#6
52	I(3)	A(1)	S(3)	12.0	#1-#6
53	I(3)	A(2)	S(0)	0.0	NOTHING
54	I(3)	A(2)	S(1)	4.4	#1,#3,#5,#7,#9,#11
55	I(3)	A(2)	S(2)	8.8	#2,#4,#6,#8,#10,#12
56	I(3)	A(2)	S(3)	13.2	#1-#12
57	I(3)	A(3)	S(0)	0.0	NOTHING
58	I(3)	A(3)	S(1)	5.2	#1,#3,#5,#7,#9,#11,#13,#15,#17
59	I(3)	A(3)	S(2)	10.4	#2,#4,#6,#8,#10,#12,#14,#16,#18
60	I(3)	A(3)	S(3)	15.6	#1-#18
61	I(3)	A(4)	S(0)	0.0	NOTHING
62	I(3)	A(4)	S(1)	6.8	#1,#3,#5,#7,#9,#11,#13,#15,#17,#19,#21,#23
63	I(3)	A(4)	S(2)	13.6	#2,#4,#6,#8,#10,#12,#14,#16,#18,#20,#22,#24
64	I(3)	A(4)	S(3)	20.4	#1-#24

FIG. 12A

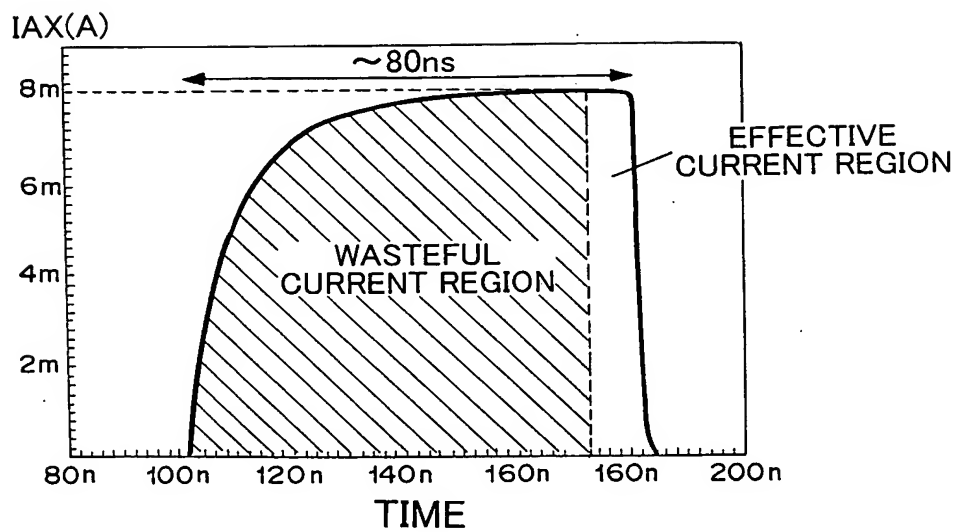


FIG. 12B

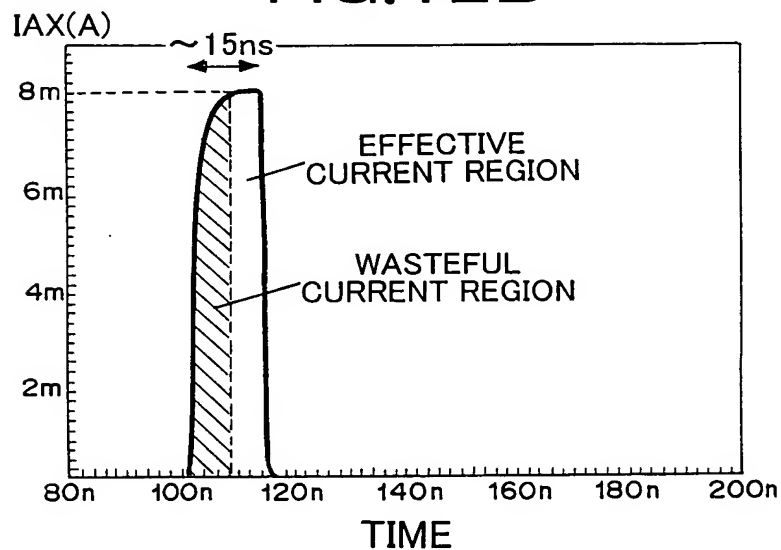


FIG. 13

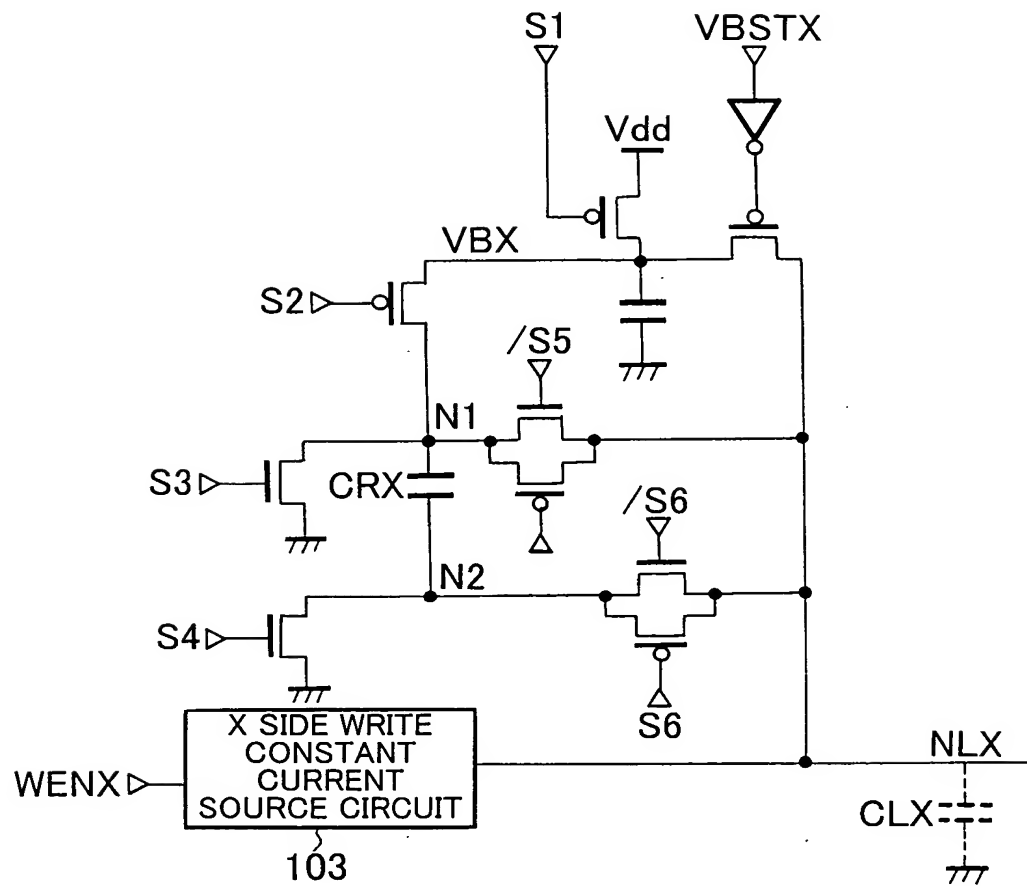


FIG. 14

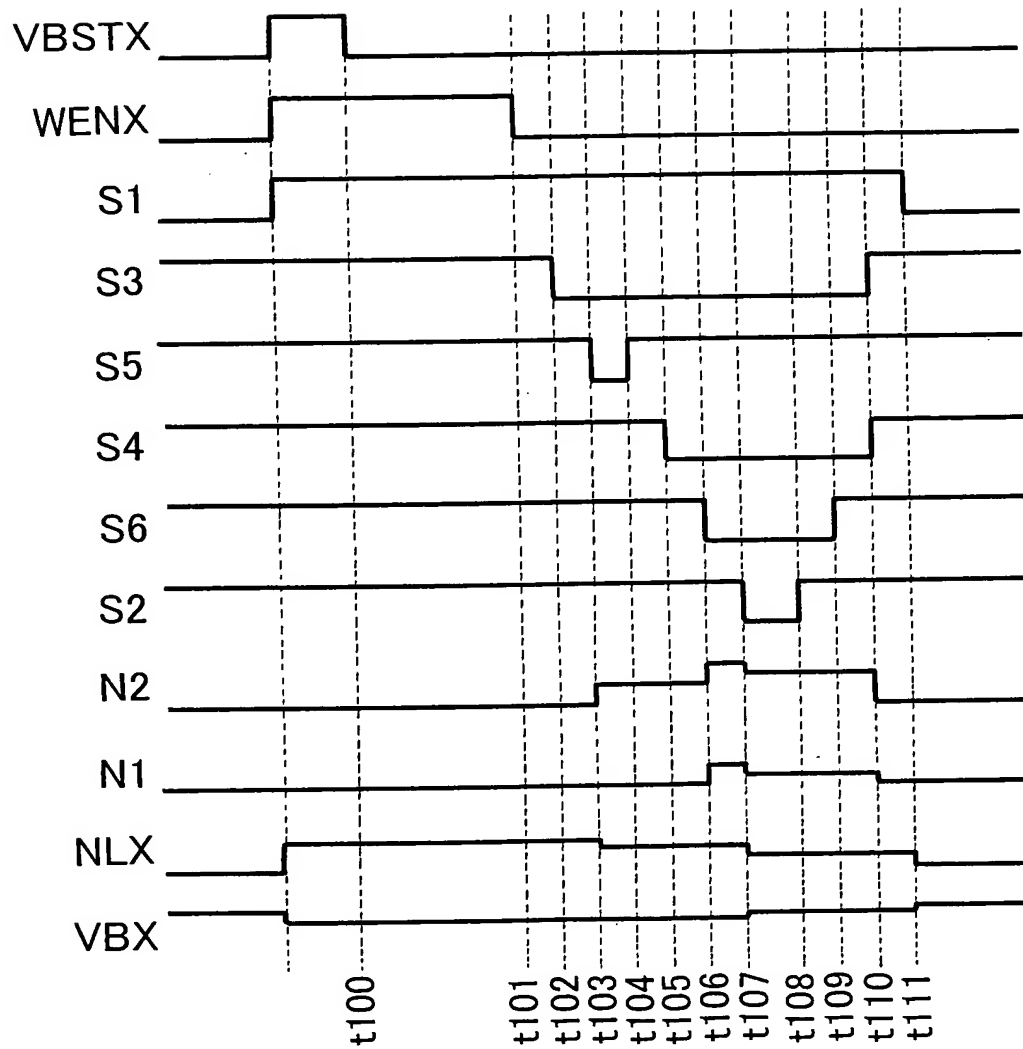


FIG. 15

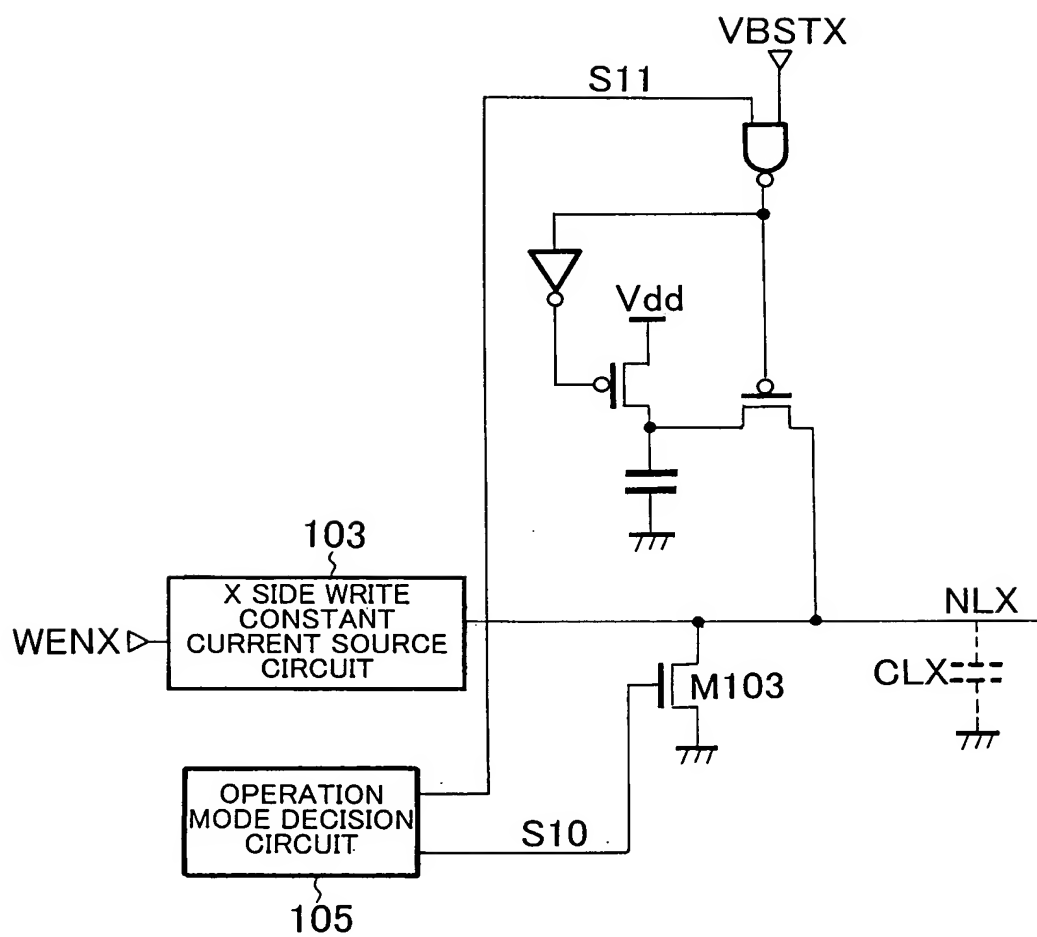


FIG. 16

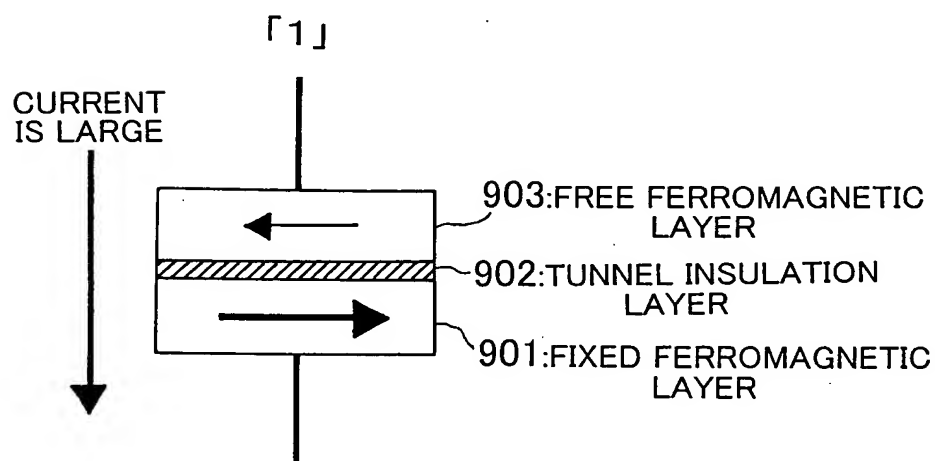
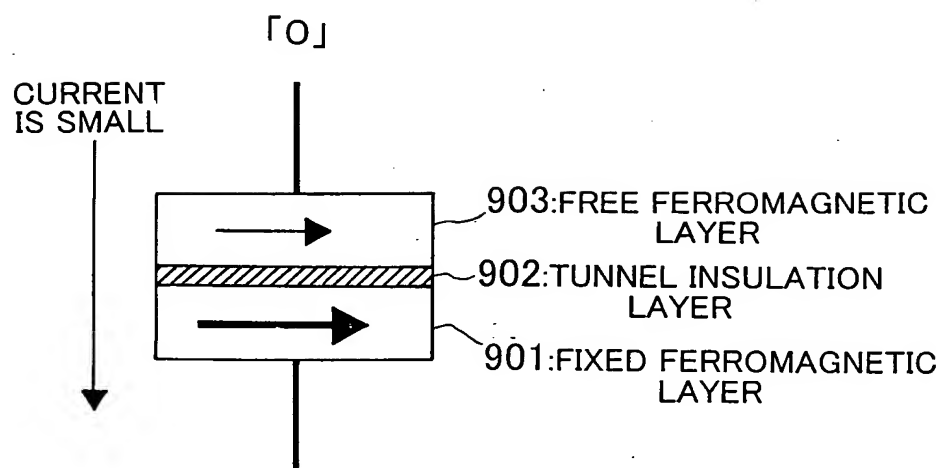


FIG. 17A

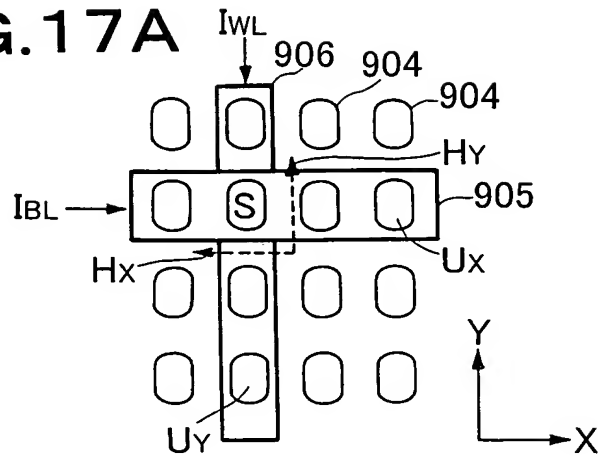


FIG. 17B

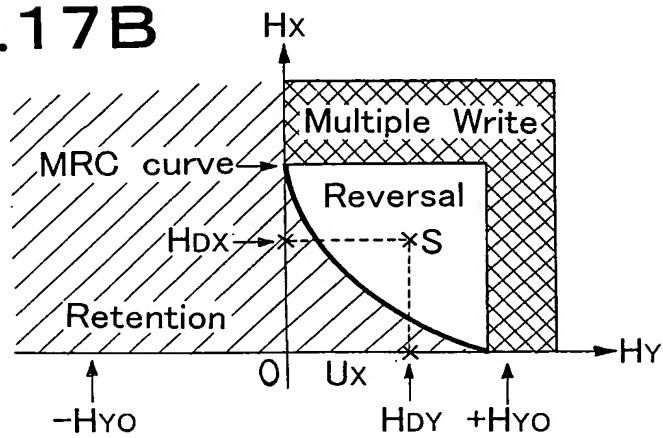


FIG. 17C

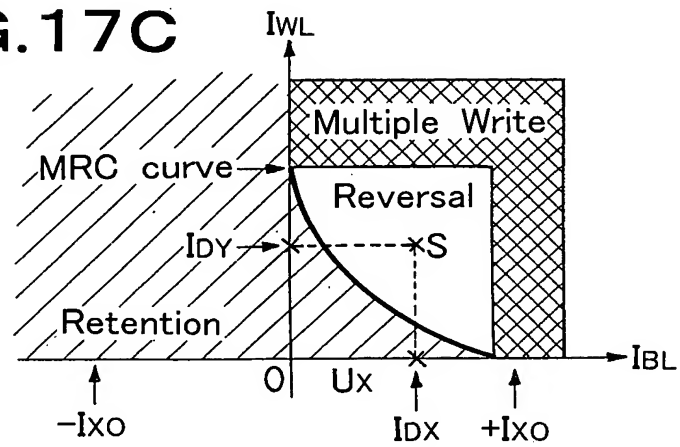
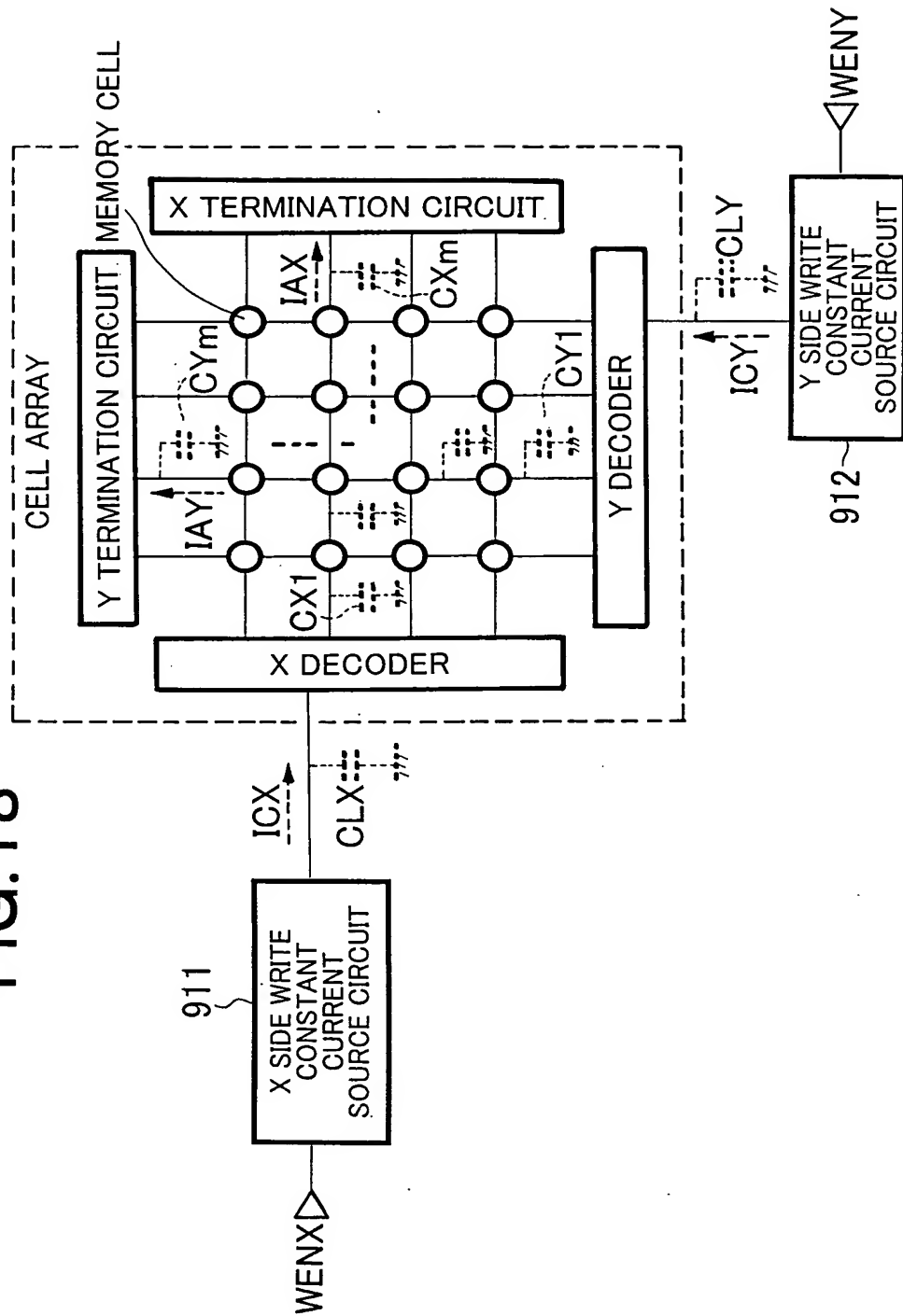


FIG. 18



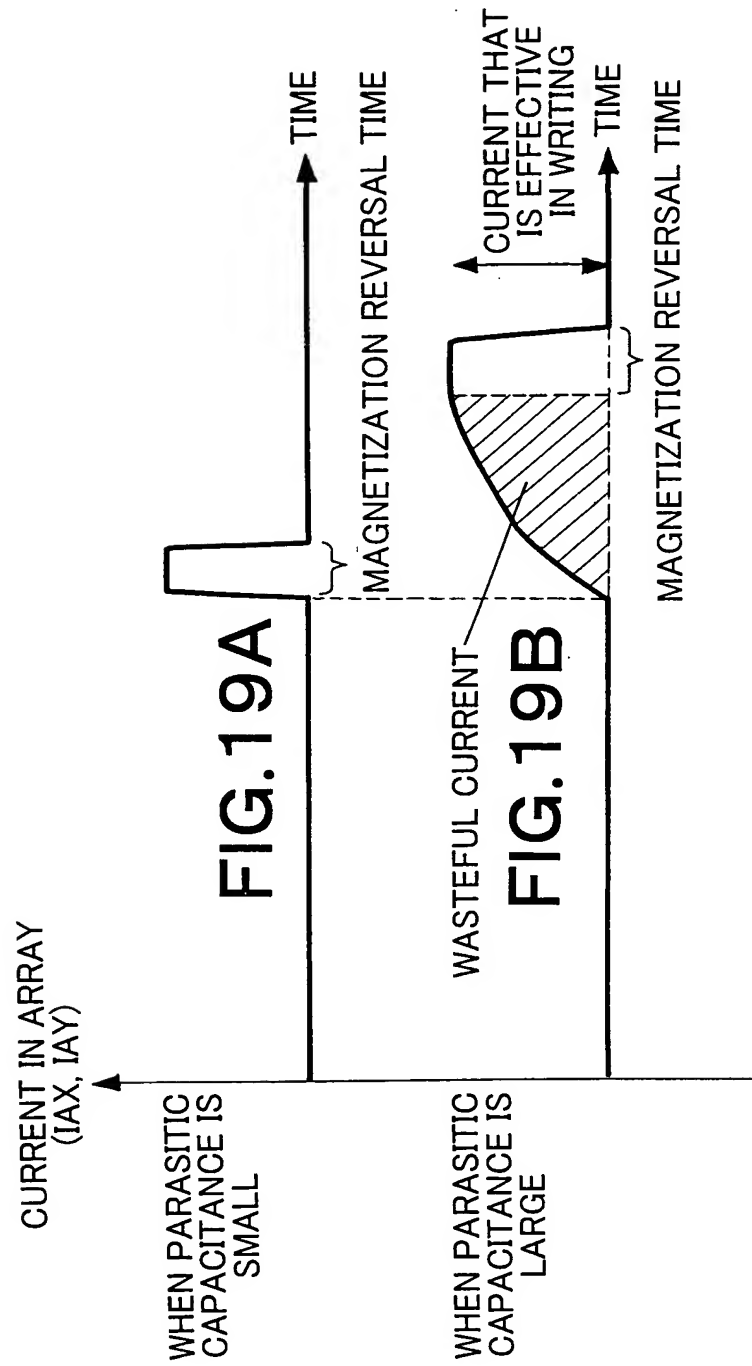


FIG. 20

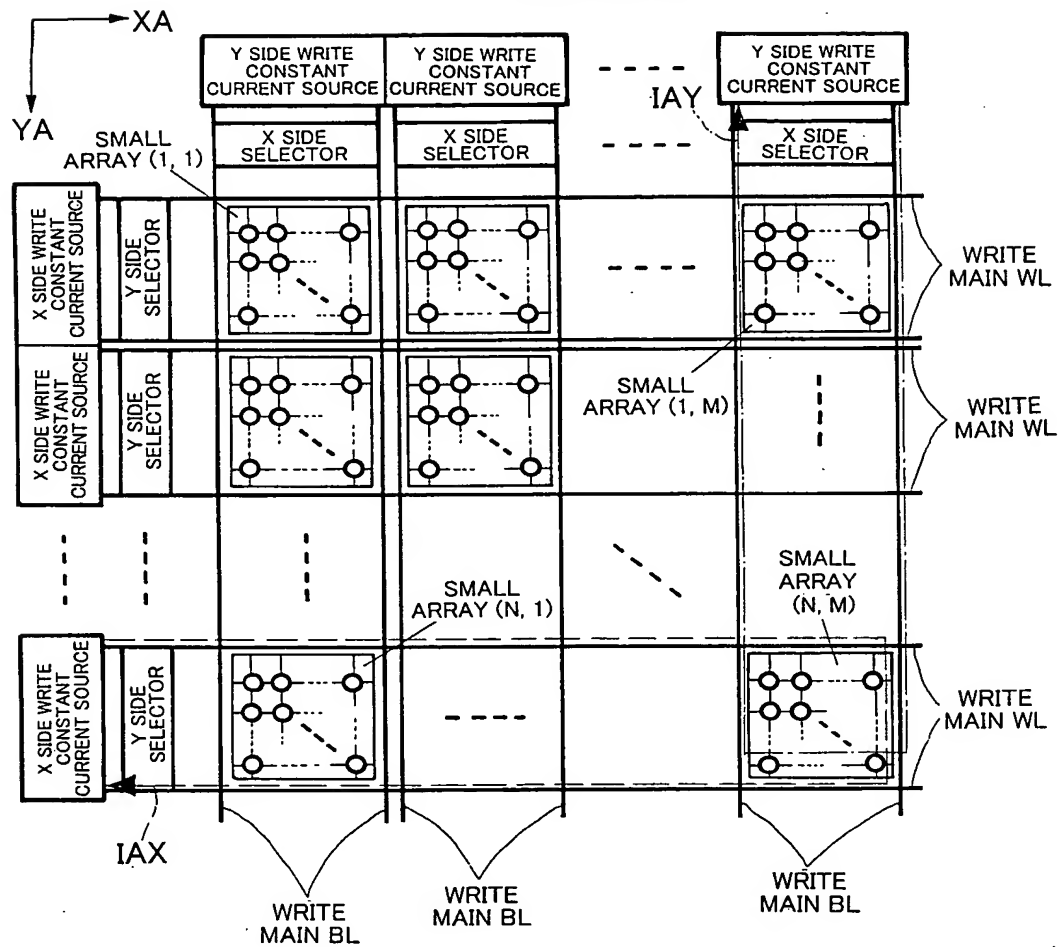


FIG. 21

